REMARKS

This is in response to a non-final Office Action dated June 7, 2004. Claims 1, 3-13 and 15-21 are pending in the application. Applicant respectfully traverses and requests reconsideration.

Summary of Rejections

Claims 1, 3-13 and 15-21 are rejected under 35 U.S.C. § 102(e) based on United States Patent No. 6,088,800 ("Jones").

Claims 1, 3-13 and 15-21 are rejected under 35 U.S.C. § 103(a) based on United States Patent No. 6,266,418 (Carter) and further in view of United States Patent No. 5,958,038 (Agrawal).

Amendments to the Claims

New claims 22 and 23 are supported by original claims 1 and 3, and by the specification on page 5, line 20 through page 6, line 2.

Claim Rejection Under 35 U.S.C. §102

Claims 1, 3-13, and 15-21 are rejected under 35 U.S.C. §102(e) based on U.S. Patent No. 6,088,800 to Jones. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly, or inherently described, in a single reference. Furthermore, the identical invention must be shown in as complete detail as contained in the claim.

Jones

Jones is directed to an encryption processor with shared memory interconnect. (Jones, title.) The encryption device, integrated into a single chip, is a parallel pipelined processor system whose instruction set is optimized for common encryption algorithms. (Jones, col. 3, lines 32-35.) As shown in Fig. 2 of Jones, the pipeline is made up of a plurality of processing elements 37 arranged in a linear array, each containing an instruction memory, a register file, and ALU, local and shared data memory, and control circuitry. (Jones col. 6, lines 10-13) Processing element 37 consists of an ALU 56 operating on 32 bit words from a register file 58 made up of 8-16 32-bit registers. (Jones col. 7, lines 17-19). The register file 58 and ALU 56 are controlled by a control unit 60 which decodes instructions from a processing element

instruction memory 62. (Jones col. 7, lines 19-22). Each processing element instruction memory stores at least one round of an encryption algorithm, where a round is defined as a sequence of instructions in an encryption algorithm. (Jones col. 7, lines 22-25). The basic concept behind DES, as illustrated in Fig. 14, consists of a substitution followed by a permutation on the text based on the key. (Jones, col. 17, lines 3-5.) The 64-bit block is divided into two 32-bit pieces 108, 110. (Jones, col. 17, lines 7-8.) One piece is unaffected by the encryption. (Jones, col. 17, lines 8-9.) The piece that is affected is divided into eight groups of four bits. (Jones, col. 17, lines 10-11.) Each group is expanded by coping the two bits adjacent to it. (Jones, col. 17, lines 11-12.) Each expanded group is XOR'ed at 112 with a subkey. (Jones, col. 17, line 14.) The six-bit result of the XOR is used to indicate a 64-entry X 4-bit. (Jones, col. 17, lines 15-17.)

Applicants submit that Jones fails to disclose each and every element of Applicants' claimed subject matter and respectfully request the Examiner to withdraw the rejections. In addition, Applicants submit that Jones does not, disclose, teach or suggest, either implicitly or explicitly, Applicants' claimed subject matter.

Claim 1

Applicants submit that Jones does not disclose, teach or suggest Applicants' amended claim 1 subject matter including, inter alia,:

> "...an arithmetic logic unit having a logic circuit for performing expansion permutation, S-box substitution, P-box permutation and associated XOR operations; wherein said computer system further comprises a register file providing operands to said arithmetic logic unit; and wherein said register file includes general purpose registers"

(claim 1). Applicants submit that Jones is absent any disclosure, teaching or suggestion regarding, inter alia, "...wherein said computer system further comprises a register file providing operands to said arithmetic logic unit; and wherein said register file includes general purpose registers." Applicants have carefully reviewed the Office Action's reference to (Jones, col. 6, lines 3-13; col. 7, lines 15-38; col. 16, line 57 through col. 18, line 13; and figures 2, 4, 5, 6 and 14), which is alleged to disclose "a register file providing operands to said arithmetic logic unit," and find no disclosure to the use of a general purpose registers for providing of operands to an arithmetic logic unit. Further, Applicants submit that which is disclosed at (Jones, col. 7, lines 15-38) is limited to providing 32-bit words from a register file 58 is absent any discussion of the

use of general purpose registers as claimed. In contrast, the registers that are discussed in Jones, as cited, col. 7, lines 17-21, are limited to providing 32-bit words to ALU56.

The disclosure in Jones is teaching an array of processing elements at column 3, lines 45 through 66, is precisely the prior art described in the Background of the invention in the instant application. For example, the Background of the invention states:

> as the encryption/decryption process of the DES algorithm of FIG. 1 is too computationally demanding for a software implementation on a general purpose microprocessor, the DES algorithm is often implemented by *an array of identical special purpose modules* outside of the microprocessor. However, several drawbacks are inheriting such an approach. First, partitioning the encryption/decryption tasks between the microprocessor and the special purpose modules is complex, especially since the different instruction sets are executed by the microprocessor and the special purpose modules.

(Specification, page 3, lines 25-35 (emphasis added).) Rather, the DES algorithm is implemented without the special purpose modules of the prior art. (Specification, page 4, lines 31-33.) For example, the DES algorithm may be implemented on a general purpose microprocessor while storing the states of the DES algorithm in general purpose registers, rather than, special purpose modules of the prior art. (Specification, page 5, lines 20-30.) A general purpose register is usually explicitly addressable, with any set of registers, that can be used for different purposes, for example, as an accumulator, as an index register, or as a special handler of video. As such, Applicants submit that Jones's disclosed use of ALU 56 operating on 32-bit words from the register file 58 does not disclose, teach or suggest applicants claimed subject matter including at least "wherein said register file includes general purpose registers."

Claim 3

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 3 subject matter including, inter alia:

> "... said register file includes a first register for storing a first portion of a datum for said encryption or decryption, a second register for storing a second portion of said datum and a third register for storing a subkey"

(claim 3). The Office Action makes reference to the same stated language in Jones at col. 6, lines 3-13; col. 7, lines 15-38; col. 16 lines 57 to col. 18, line 13 and figures 2, 4, 5, 6 and 14 as disclosing Applicant's claim 3 subject matter. The Examiner's repeated block citation to Jones

in reference to rejecting each and every element of all the claims fails to show the particular part in Jones relied on and fails therefore to provide the alleged limitation by limitation analysis of the claims and also fails to show the part of Jones relied on for the rejections as required by 37 C.F.R. § 1.104(c)(2)[1]. Applicants submit that what Jones discloses in Jones at col. 6, lines 3-13; col. 7, lines 15-38; col. 16 lines 57 to col. 18, line 13 and figures 2, 4, 5, 6 and 14 is a description of *inter alia* of ALU 56 operating in 32-bit words from the register file 58 with 16 by 32-bit registers. (Jones col. 7, lines 17-19). As a result, Jones as cited is absent any discussion of using a first, second and third register in the manner claimed in Applicants' claim 3 subject matter. Therefore, the Applicants hereby request a showing of where Jones teaches each and every element as arranged in the claims. Further, the Office Action fails to show where Jones teaches 'a third register for storing a subkey." In addition, and as discussed above in regards to claim 1, Jones's discussion in col. 7, lines 17-20 is directed to merely *inter alia* ALU 56 receiving 32-bit words from a register file and as such there is no discussion therein using a first, second and third register in the manner claimed in Applicants' claimed subject matter. Therefore, Applicants submit that Jones does not disclose, teach or suggest Applicants' claimed subject matter.

Applicants submit that at least because claim 3 depends from claim 1, and as a dependent claim therefrom, claim 3 is allowable for the reasons claim 1 is allowable. Applicants further submit that claim 3 is also allowable in light of the presence of novel and non-obvious elements contained in claim 3 that are not otherwise present in claim 1.

Claim 4

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 4 subject matter including, inter alia,: "... said datum is 64 bits long and said subkey is 48 bits long" (claim 4). In contrast, Jones teaches that the ALU 56 receives 32-bit words from register file 58 and therefore teaches away from the claimed subject matter "... said datum is 64 bits long and said subkey is 48 bits long." Again, the Office Action fails to show where Jones teaches among other things "... said datum is 64 bits long and said subkey is 48 bits long."

Applicants submit that at least because claim 4 depends from claim 3, and as a dependent claim therefrom, claim 4 is allowable for the reasons claim 3 is allowable. Applicants further

[1] When the reference is complex or shows or describes inventions other than that claimed by the applicant, a particular part relied on must be designated as nearly as practicable 37 C.F.R. § 1.104(c)(2).

submit that claim 4 is also allowable in light of the presence of novel and non-obvious elements contained in claim 4 that are not otherwise present in claim 3.

Claim 5

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 5 subject matter including, inter alia,: "... said first and second portions each contain one-half number of bits of said datum" (claim 5). Applicants repeat the relevant remarks made above. Again, the Office Action fails to show where Jones teaches each and every element as arranged in the claims. The Office Action again merely cites generally to the same portions of Jones without showing where the each and every element as arranged in the claims is taught in Jones.

Applicants submit that at least because claim 5 depends from claim 3, and as a dependent claim therefrom, claim 5 is allowable for the reasons claim 3 is allowable. Applicants further submit that claim 5 is also allowable in light of the presence of novel and non-obvious elements contained in claim 5 that are not otherwise present in claim 3.

Claim 6

Applicants submit that Jones does not disclose, teach or suggest applicants claim 6 subject matter including "wherein each of said first and second portions is 32-bits long." Again, the Office Action cites generally to the same portions of Jones without showing where each and every element as arranged in the claims is taught in Jones. Applicants repeat the relevant remarks made above.

Applicants submit that at least because claim 6 depends from claim 5, and as a dependent claim therefrom, claim 6 is allowable for the reasons claim 5 is allowable. Applicants further submit that claim 6 is also allowable in light of the presence of novel and non-obvious elements contained in claim 6 that are not otherwise present in claim 5.

Claim 7

Applicants cannot find where Jones discloses, teaches or suggests Applicants' claim 7 subject matter including, inter alia:

> "... said first, second and third registers store operands of an instruction executing one round of said DES algorithm using said logic circuit and a shift circuit in said arithmetic logic unit, said instruction designating to store results in said first, second and third registers in such manner as to allow said results in said first, second and third registers to be operands in a subsequent executing of said instruction."

(claim 7). Here, the Office Action again makes reference to the stated language in Jones without showing where Jones teaches each and every element as arranged in the claims. Applicants again repeat the above relevant remarks, in particular those remarks directed to the second and third registers. Further, the Office Action fails to show where Jones teaches "... said first, second and third registers store operands of an instruction executing one round of said DES algorithm using said logic circuit and a shift circuit in said arithmetic logic unit, said instruction designating to store results in said first, second and third registers in such manner as to allow said results in said first, second and third registers to be operands in a subsequent executing of said instruction."

Applicants submit that at least because claim 7 depends from claim 3, and as a dependent claim therefrom, claim 7 is allowable for the reasons claim 3 is allowable. Applicants further submit that claim 7 is also allowable in light of the presence of novel and non-obvious elements contained in claim 7 that are not otherwise present in claim 3.

Claim 8

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 8 subject matter including, inter alia,: "... a bypass mechanism is provided in said register file such that said results are provided as input to said logic circuit without first being written back to said first, second and third registers" (claim 8). Again, the Office Action makes reference to the stated language in Jones previously cited as disclosing Applicant's claimed subject matter without showing where Jones teaches each and every element in the claims. As discussed above, not only is such language in Jones absent from any discussion of the use of a register file containing general purpose registers, or first, second and third general purpose registers, Applicants further submit that Jones is also absent discussion on the use of Applicant's claimed bypass mechanism 302–Fig. 3. Therefore, Applicants submit that Jones cannot and does not disclose, teach or suggest Applicant's claimed subject matter. Although the arguments previously argued that Jones does not teach the claimed bypass mechanism, the final Office Action dated June 7, 2004 fails to address the applicants previous argument. As a result, the Office Action again fails to show where Jones teaches each and every element as arranged in the claims. Again, applicants respectfully request that the Examiner provide such a showing or to at

least address applicants arguments. Therefore, the Applicants respectfully request that the Examiner withdraw the rejection requirement of the Office Action dated June 7, 2004 since the Examiner failed to both address the Applicants previous arguments and to show where Jones teaches each and every element of the claims as required by 37 C.F.R. § 1.104(c)(2).

Applicants submit that at least because claim 8 depends from claim 7, and as a dependent claim therefrom, claim 8 is allowable for the reasons claim 7 is allowable. Applicants further submit that claim 8 is also allowable in light of the presence of novel and non-obvious elements contained in claim 8 that are not otherwise present in claim 7.

Claim 9

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 9 subject matter including, inter alia,: "... said register file and said bypass mechanism are shared by all instructions in said arithmetic logic unit" (claim 9). Regarding the same cited language in Jones at col. 6, lines 3-13; col. 7, lines 15-38; col. 16 lines 57 to col. 18, line 13 and figures 2, 4, 5, 6 and 14, Applicants submit that Jones discusses a DES operation generally at col. 16, lines 57 through col. 18 lines 13, but is otherwise absent any discussion of a "bypass mechanism," and therefore does not disclose Applicants' claimed subject matter. Applicants repeat the relevant remarks made above. Again, Applicants previously made the above argument in the previous response; however, the Office Action yet again fails to address Applicants arguments. As such, the Applicants respectfully request withdrawal of the finality of the Office Action of June 7, 2004 since the Office Action fails to address the Applicants previous arguments and fails to show how Jones teaches each and every element as arranged in the claims pursuant to 37 C.F.R. § 1.104(c)(2). At least for such reasons, Applicants submit that Jones does not teach or disclose or suggest Applicants Claim 9 subject matter.

Further, Applicants submit that at least because claim 9 depends from claim 8, and as a dependent claim therefrom, claim 9 is allowable for the reasons claim 8 is allowable. Applicants further submit that claim 9 is also allowable in light of the presence of novel and non-obvious elements contained in claim 9 that are not otherwise present in claim 8.

Claim 10

Applicants repeat the relevant remarks made above. Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 10 subject matter including, inter alia,:

"... a second logic circuit capable of performing key selection for said DES algorithm, said second logic circuit operation in parallel with said logic circuit."

(claim 10). Here, the Office Action again makes reference to the same cited portions of Jones made with all the other claims in the Office Action as disclosed in Applicants claim 10 subject matter. Applicants submit that Jones at col. 16, line 57 through col. 18, line 14 discloses a DES system generally, however the Office Action fails to show where Jones teaches "... a second logic circuit capable of performing key selection for said DES algorithm, said second logic circuit operation in parallel with said logic circuit." Further, the cited portion of Jones teaches DES creates subkeys from a single key, in this case 56-bits. However, the Applicants are unable to find where Jones although discussing the creation of subkeys fails to disclose performing of a key selection parallel with the logic circuit. Therefore, Applicant submits that Jones cannot and does not disclose, teach or suggest Applicants claimed subject matter.

Applicants submit that at least because claim 10 depends from claim 1, and as a dependent claim therefrom, claim 10 is allowable for the reasons claim 1 is allowable. Applicants further submit that claim 10 is also allowable in light of the presence of novel and non-obvious elements contained in claim 10 that are not otherwise present in claim 1.

Claim 11

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 11 subject matter including, inter alia,: "... said logic circuit further comprises a circuit for selecting a subkey from a key" (claim 11). Applicants repeat the relevant remarks made above.

Applicants submit that at least because claim 11 depends from claim 1, and as a dependent claim therefrom, claim 11 is allowable for the reasons claim 1 is allowable. Applicants further submit that claim 11 is also allowable in light of the presence of novel and non-obvious elements contained in claim 11 that are not otherwise present in claim 1.

Claim 12

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 12 subject matter including, inter alia,: "... said key is 56 bits long" (claim 12). Applicants repeat the relevant remarks made above.

Applicants submit that at least because claim 12 depends from claim 11, and as a dependent claim therefrom, claim 12 is allowable for the reasons claim 11 is allowable.

Applicants further submit that claim 12 is also allowable in light of the presence of novel and non-obvious elements contained in claim 12 that are not otherwise present in claim 11.

Claim 13

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 13 subject matter including, inter alia, "wherein said register file includes general purpose registers." (claim 13). Applicants submit that for the same reasons discussed above regarding the reasons why Jones does not disclose, teach or suggest Applicants' claim 1 subject matter, that Jones also does not disclose, teach or suggest Applicants' claim 13 subject matter. Namely, Applicants submit that Jones does not disclose, teach or suggest the use of "wherein said register file includes general purpose registers." Therefore, Applicants submit that Jones cannot and does not disclose, teach or suggest Applicant's claimed subject matter.

Claim 15

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 15 subject matter including, inter alia,: "... storing operands in a register file; and providing said operands to said logic circuit." (claim 15).

Applicants submit that for the same or similar reasons discussed above regarding the reasons why Jones does not disclose, teach or suggest Applicants' claim 2 subject matter, that Jones also does not disclose, teach or suggest Applicants' claim 15 subject matter. Therefore, Applicants submit that Jones cannot and does not disclose, teach or suggest Applicants' claimed subject matter.

Applicants submit that at least because claim 15 depends from claim 13, and as a dependent claim therefrom, claim 15 is allowable for the reasons claim 13 is allowable. Applicants further submit that claim 15 is also allowable in light of the presence of novel and non-obvious elements contained in claim 15 that are not otherwise present in claim 13.

Claim 16

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 16 subject matter including, inter alia,:

> "... storing a first portion of a datum for said encryption or decryption in first register in said register file; storing a second portion of said datum for said encryption or decryption in second register in said register file; and storing a subkey for said encryption or decryption in third register in said register file."

(claim 16). Applicants submit that for the same or similar reasons discussed above regarding the reasons why Jones does not disclose, teach or suggest Applicants' claim 3 subject matter, that Jones also does not disclose, teach or suggest Applicants' claim 16 subject matter. Therefore, Applicants submit that Jones cannot and does not disclose, teach or suggest Applicants' claimed subject matter.

Applicants submit that at least because claim 16 depends from claim 15, and as a dependent claim therefrom, claim 16 is allowable for the reasons claim 15 is allowable. Applicants further submit that claim 16 is also allowable in light of the presence of novel and non-obvious elements contained in claim 16 that are not otherwise present in claim 15.

Claim 17

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 17 subject matter including, inter alia,:

> "... storing operands of an instruction executing on e round of said DES algorithm in said first, second and third registers using said logic circuit and said shift circuit, said instruction designating to store results in said first, second and third registers in such manner as to allow said results in said first, second and third registers to be operands in a subsequent execution of said instruction."

(claim 17). Applicants submit that for the same or similar reasons discussed above regarding the reasons why Jones does not disclose, teach or suggest Applicants' claim 7 subject matter, that Jones also does not disclose, teach or suggest Applicants' claim 17 subject matter. Therefore, Applicants submit that Jones cannot and does not disclose, teach or suggest Applicants' claimed subject matter.

Applicants submit that at least because claim 17 depends from claim 16, and as a dependent claim therefrom, claim 17 is allowable for the reasons claim 16 is allowable. Applicants further submit that claim 17 is also allowable in light of the presence of novel and non-obvious elements contained in claim 17 that are not otherwise present in claim 16.

Claim 18

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 18 subject matter including, inter alia,: "... providing said results as input to said logic circuit without first being written back to said first, second and third registers." (claim 18).

Applicants submit that for the same or similar reasons discussed above regarding the reasons why Jones does not disclose, teach or suggest Applicants' claim 8 subject matter, that Jones also does not disclose, teach or suggest Applicants' claim 18 subject matter. Therefore, Applicants submit that Jones cannot and does not disclose, teach or suggest Applicants' claimed subject matter.

Applicants submit that at least because claim 18 depends from claim 17, and as a dependent claim therefrom, claim 18 is allowable for the reasons claim 17 is allowable. Applicants further submit that claim 18 is also allowable in light of the presence of novel and non-obvious elements contained in claim 18 that are not otherwise present in claim 17.

Claim 19

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 19 subject matter including, inter alia,: "... selecting a subkey from a key for said DES algorithm in a second logic circuit." (claim 19). Applicants repeat the above relevant remarks.

Applicants submit that at least because claim 19 depends from claim 13, and as a dependent claim therefrom, claim 19 is allowable for the reasons claim 13 is allowable. Applicants further submit that claim 19 is also allowable in light of the presence of novel and non-obvious elements contained in claim 19 that are not otherwise present in claim 13.

Claim 20

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 20 subject matter including, inter alia,: "... operating said second logic circuit in parallel with said logic circuit." (claim 20). Applicants repeat the above relevant remarks.

Applicants submit that for the same or similar reasons discussed above regarding the reasons why Jones does not disclose, teach or suggest Applicants' claim 10 subject matter, that Jones also does not disclose, teach or suggest Applicants' claim 20 subject matter. Therefore, Applicants submit that Jones cannot and does not disclose, teach or suggest Applicants' claimed subject matter.

Applicants submit that at least because claim 20 depends from claim 19, and as a dependent claim therefrom, claim 20 is allowable for the reasons claim 19 is allowable. Applicants further submit that claim 20 is also allowable in light of the presence of novel and non-obvious elements contained in claim 20 that are not otherwise present in claim 19.

Claim 21

Applicants submit that Jones does not disclose, teach or suggest Applicants' claim 21 subject matter including, inter alia, "... selecting a subkey from a key using a key select circuit in said logic circuit." (claim 21). Applicants repeat the above relevant remarks.

Applicants submit that at least because claim 21 depends from claim 13, and as a dependent claim therefrom, claim 21 is allowable for the reasons claim 13 is allowable. Applicants further submit that claim 21 is also allowable in light of the presence of novel and non-obvious elements contained in claim 21 that are not otherwise present in claim 13.

Claims 22 and 23

Applicants repeat the above relevant remarks New claim 22 recites, among other things, "wherein said register file includes general purpose registers to store at least two of attributes parameters datapath, control, L_i's, R_i's, and subkeys K_i's." In contrast, Jones teaches that the register file 58 is controlled by control unit 60, which decodes instructions from a processing element instruction memory 62. As such, the register file does not store at least two of attributes parameters datapath, namely control, L_i's, R_i's, and subkeys K_i's.

Applicants submit that at least because claim 21 depends from claim 13, and as a dependent claim therefrom, claim 21 is allowable for the reasons claim 13 is allowable. Applicants further submit that claim 21 is also allowable in light of the presence of novel and non-obvious elements contained in claim 21 that are not otherwise present in claim 13

Claim Rejection Under 35 U.S.C. §103

Claims 1, 3-13 and 15-21 are rejected under 35 U.S.C. § 103(a) based on United States Patent No. 6,26,418 (Carter) and further in view of United States Patent No. 5,958,038 (Agrawal). Applicants repeat the above relevant remarks

The Office Action acknowledges that "Carter" fails to specifically teach the computer system as an arithmetic logic unit (ALU) and the register file with general purpose registers (GPR's). (Office Action page 7).

According to the cited portion of Carter, Carter teaches "preferably, the cryptographic algorithm that SCS 100 implies is the triple DES 64-bit codebook." Triple DES is a three pass, sixteen-round, substitution-permutation network cryptosystem (a Fiestel Cypher) and has a block

size of 64-bits, and uses up to an 868 bit key. (Col. 5, lines 51-55). Triple DES uses standard arithmetic medical and logical operators along with an expansion permutation, and S-box substitution, and a P-box permutation per round. (Carter Col. 5, lines 55-58). Accordingly, the cited portion of Carter is limited to describing standard arithmetic medical and logical operators with an expansion permutation and S-box substituting an a P-box permutation, rather than, "wherein said computer system further comprises a register file providing an arithmetic logic unit; and wherein said register file includes general purpose register." (Claim 1). The cited portion of Carter at col. 8, lines 6-18 which states "the negotiation signaling also allows the SCs to choose the public key module size (e.g., 512 bits, 1024 bits, 2048 bits, 3096 bits), the source of the module is (e.g., SKIP protocol, custom develop, etc.) and the length of the traffic (e.g., 56 bits, 64 bits, 80 bits, 112 bits, 128 bits, 168 bits, etc.) is merely limited to describing negotiation signaling rather than the claimed subject matter including "wherein said computer system further comprises a register file providing an arithmetic logic unit; and wherein said register file includes general purpose register." The cited portion of Agrawal at col. 2, lines 15-24 which states:

> "yet another approach used to increase processing efficiency is the very long word (VLIW) format. The VLIW format explicitly includes instruction level parallelism into a very long instruction word. The VLIW typically has fields for frequently performed operations, such as ALU operations and memory accesses. By using VLIW, the instructions required for a DSP filter can be incorporated into a single instruction word. Moreover, the VLIW format allows use of a low complexity decoder and has the potential for high performance by paralyzing the use of multiple functional units within the processor."

(Agrawal col. 2, lines 15-24) However, such language in Agrawal is merely limited to the use of a very long instruction word format rather than "wherein said computer system further comprises a register file providing an arithmetic logic unit; and wherein said register file includes general purpose register." Even though the Office Action acknowledges that Carter fails to specifically teach the computer system as an arithmetic logic unit and a register file with general purpose registers, no where does the Office Action show where Agrawal makes up for Carter's shortcomings. For example, no where does the Office Action even assert that Agrawal even teaches "wherein said computer system further comprises a register file providing an arithmetic logic unit; and wherein said register file includes general purpose registers." As such, the

combination of Carter and Agrawal, to the extent that can be combined, would merely teach a triple DES arithmetical and logical operators along with an expansion permutation which uses the VLIW format. As such, the combination of Carter and Agrawal fails to teach each and every element as arranged in the claims even if combined.

Finally, the Office Action fails to show any sufficient motivation for modifying Carter with the teachings of Agrawal. As such, the Office Action fails to show for example Agrawal as directed to "computer processor with two addressable memories and two streamed registers and method of data streaming of operation." (Agrawal, title). This being the case, one would not be motivated to modify Carter with Agrawal since Agrawal is directed to solving a completely different problem than Carter is. As such, the Office Action fails to show sufficient motivation for modifying Carter with Agrawal and therefore the Office Action fails to establish a *prima facie* case of obviousness.

With regards to claims 3-22 and 15-21 the Office Action broadly makes reference to Carter col. 5, lines 51-61 and col. 8, lines 6-18 for teaching each and every element for each of these claims. As stated above, the Office Action yet again fails to show and specifically point out where the combination of Carter and Agrawal teach each and every element as arranged in the claims pursuant to 37 C.F.R. § 1.104(c)(2) as such the Office Again fails to establish a *prima facie* case of obviousness for each and every element of each of these claims. Applicants request a corresponding showing of. Applicant submits that at least because at least the dependent depend from an independent claim or an intermediate claim therewith, the dependent claims are allowable for at least the reasons that the independent claims are allowable. Applicants further submit that claims 3-12 and 15-21 are allowable in light of the presence of novel and non-obvious elements contained in those claims that are not otherwise present in the independent claims.

CONCLUSION

For the foregoing reasons, withdrawal of the rejections and allowance of the claims is respectfully requested. If there are any questions or comments regarding this response the Examiner is encouraged to contact the undersigned at 312-609-7970.

Respectfully submitted,

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